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ABSTRACT OF DISCLOSURE

A PDP apparatus of low power consumption and without erroneous malfunctions is equipped with a sustaining circuit that prevents an on/off timing shift and deterioration of a sustaining pulse produced thereby. Phase adjusting circuits, which adjust the timing of the changing edge of the sustaining pulse, are provided for the sustaining circuit; the power recovery circuit is of improved efficiency; and power consumption is reduced by optimizing the timing of a changing edge of the sustaining pulse The circuit devices used in the sustaining circuits are classified according to delay times and sets of the circuit devices are selected so that the timing of a changing edge of the sustaining pulse falls within a predetermined allowance, and the selected sets of the circuit devices are set to the PDP.